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EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,465	GINSBERG, MICHAEL	
	Examiner	Art Unit	
	Syed J. Ali	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-13,15-20 and 22-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13,15-20 and 22-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed July 6, 2005. Claims 1-6, 8-13, 15-20, and 22-29 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 103

3. **Claims 1-6, 8-13, 15-20, and 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toll et al. (U.S. Patent No. 6,308,279) (hereinafter Toll) in view of Fung (U.S. Patent No. 6,584,571).**

4. As per claim 1, Toll teaches the invention as claimed, including a method for providing thread scheduling in a device, the device comprising one or more hardware elements operatively coupled to an operating system comprising a plurality of program modules, the method comprising:

scheduling one or more threads according to a predetermined periodic rate (col. 3 lines 38-45; col. 4 lines 58-63);

determining whether or not there are any threads to execute (col. 2 lines 32-34; col. 3 lines 8-12); and

responsive to a determination that there are no threads to execute, deactivating one or more of the hardware elements and the program modules for a dynamic variable amount of time

(col. 2 lines 32-34; col. 3 lines 8-12, 23-30), the dynamic variable amount of time being independent of the predetermined periodic rate (col. 3 lines 16-18).

5. Fung teaches the invention as claimed, including deactivating a group of components in response to an absence of executing threads for a dynamically variable amount of time based on a sleep state of a set of threads (col. 6 lines 14-30; col. 6 lines 45-51).

6. First, it is noted that neither Toll nor Fung describe idle or sleeping threads being stored in a sleep queue. However, this is a well-known feature of thread scheduling. For example, Zolnowsky (USPN 6,779,182) describes a prior art method of storing blocked threads awaiting synchronization in a sleep queue (Fig. 1B). The main focus of the claimed invention does not appear to be the storing of inactive or blocked threads in a sleep queue, but rather controlling the amount of time that the hardware elements and/or program modules are deactivated based on the activity of the system.

Toll and Fung are both directed to power conservation by means of deactivating components of a system during periods of inactivity, i.e. when there are no threads to execute. Toll places a processor in low-power mode when some of the threads are sleeping and entering a deeper power-conserving mode when all the threads are sleeping, while returning to an active power mode when a "break event" is sensed. However, Toll does not describe this "break event" with specificity, so it could be read as any of a number of different types of events. Fung, on the other hand, teaches a similar method of power conservation, while expressly stating that returning to an active power mode is performed in response to an increased level of system activity, e.g. threads that had gone to sleep have awakened and resumed processing, or based on the expiration of a time quantum.

It would have been obvious to one of ordinary skill in the art to combine Toll and Fung since the return to an active power mode may be necessary in response to an external event, as discussed by Toll, but also in response to a thread being activated due to an available synchronization construct. Though it is arguable that Toll implicitly discloses this feature, the combination with Fung describes returning to an active power state in response to an awakening thread expressly, and therefore provides a more efficient model for conserving power.

7. As per claim 2, Fung teaches the invention as claimed, including a method as recited in claim 1, wherein the dynamic variable amount of time is based on a maximum amount of time that a thread can yield before needing to be scheduled for execution (col. 7 lines 35-38).

8. As per claim 3, Toll teaches the invention as claimed, including a method as recited in claim 1, wherein the device is a battery powered device (col. 1 lines 11-24).

9. As per claim 4, the combination of Toll and Fung fails to explicitly teach the invention as claimed, including a method as recited in claim 1, wherein the operating system is a Microsoft WINDOWS CE, Linux, WindRiver, QNX, or PALM operating system. "Official Notice" is taken that the use of the claimed operating systems would have been obvious to one of ordinary skill in the art. Toll addresses the need for extending battery life in mobile computing devices (col. 1 lines 11-24). The operating system taught by Toll is taught in a more general sense, as one that supports multi-threading, and uses the scheduling of these threads as the control for

preserving battery power. Since all of the claimed operating systems are multithreaded, there is inherent support for the power mode transition method disclosed by Toll.

10. As per claim 5, Fung teaches the invention as claimed, including a method as recited in claim 1, wherein the predetermined periodic rate is a millisecond (col. 11 lines 10-14).

11. As per claim 6, Fung teaches the invention as claimed, including a method as recited in claim 1:

wherein the providing further comprises setting a system timer to generate a notification at the predetermined periodic rate (col. 7 lines 35-38);

wherein the deactivating further comprises resetting the system timer to generate the notification after the dynamic variable amount of time has elapsed since the deactivating (col. 9 lines 6-8); and

wherein the method further comprises:

receiving the notification after the dynamic variable amount of time has elapsed since the deactivating (col. 9 lines 8-13); and

responsive to the receiving:

resetting the system timer to generate the notification at the predetermined periodic rate (col. 9 lines 8-18); and

activating the one or more of the hardware modules and the program modules (col. 9 lines 16-18).

12. As per claims 8 and 9-11, Toll teaches the invention as claimed, including the method of claims 1 and 3-5, respectively, further comprising activating the one subset of components only when the operating system needs to perform an action selected from a group of actions comprising scheduling a thread for execution upon expiration of the dynamic variable amount of time since the deactivating, or upon receipt of an external event, processing the external event that is not a system timer event (col. 1 lines 25-31).

13. As per claim 12, Fung teaches the invention as claimed, including a method as recited in claim 8:

wherein the scheduling further comprises setting a system timer to the predetermined periodic rate, the predetermined periodic rate corresponding to a thread scheduling accuracy (col. 7 lines 35-38); and

wherein the deactivating further comprises resetting the system timer to generate a notification after the dynamic variable amount of time has elapsed since the deactivating (col. 9 lines 6-8).

14. As per claim 13, Fung teaches the invention as claimed, including a method as recited in claim 8:

wherein the deactivating further comprises resetting a system timer to generate a notification after the dynamic variable amount of time has elapsed (col. 9 lines 8-18), the dynamic variable amount of time being a maximum amount of time that a thread can yield to other threads before needing to be scheduled for execution (col. 7 lines 35-38); and

wherein the activating further comprises resetting the system timer to the predetermined periodic rate to provide substantial thread scheduling accuracy (col. 9 lines 16-18).

15. As per claims 15-18, Fung teaches the invention as claimed, including a computer-readable storage medium containing computer-executable instructions for performing the method of claim 1-4, respectively (Fig. 1).

16. As per claim 19, Fung teaches the invention as claimed, including a computer-readable storage medium as recited in claim 15, wherein the computer-executable instructions further comprise instructions for:

in the deactivating, configuring a system timer to send a first timer interrupt after the dynamic variable amount of time has elapsed (col. 9 lines 8-18), the dynamic variable amount of time being a maximum amount of time that a first thread can yield to a second thread before the first thread needs to be executed (col. 7 lines 35-38); and

responsive to receiving the first timer interrupt:

(a) configuring the system timer to send a second timer interrupt at the periodic rate (col. 9 lines 8-18); and

(b) activating the one or more of the program modules and the hardware elements to determine if there are any threads to execute (col. 9 lines 16-18).

17. As per claim 20, Fung teaches the invention as claimed, including a computer-readable storage medium as recited in claim 15, wherein the computer-executable instructions further comprise instructions for:

receiving an external interrupt before the dynamic variable amount of time has elapsed since the deactivating, the external interrupt not being a system timer interrupt (col. 8 lines 52-60); and

responsive to receiving the external interrupt, processing the external interrupt such that the one or more of the program modules and the hardware elements remain deactivated for the dynamic variable amount of time (col. 9 lines 8-18).

18. As per claims 22-23, 24, and 25-26, Fung teaches the invention as claimed, including a device comprising:

a processor (Fig. 1, element 4);

a plurality of hardware elements coupled to the processor (Fig. 1, elements 7-0 and 7-n); and

a memory coupled to the processor (Fig. 1, element 15), the memory comprising computer-program instructions executable by the processor, the computer-program instructions comprising a scheduler program module (col. 4 line 64 - col. 5 line 5), a hardware abstraction layer (HAL) program module (Fig. 2 element 79), one or more operating system program modules (col. 4 lines 64-66), and a set of application program modules (col. 5 lines 2-5);

wherein the scheduler comprises computer-executable instructions for performing the method of claims 1-2, 5, and 3-4, respectively.

19. As per claim 27, Fung teaches the invention as claimed, including a device as recited in claim 22, wherein the HAL further comprises computer-executable instructions for re-activating the at least one subset of components after the dynamic variable amount of time has elapsed since one or more of the program modules and the hardware elements were deactivated (col. 9 lines 16-18).

20. As per claim 28, Fung teaches the invention as claimed, including a device as recited in claim 27, wherein the scheduler is re-activated in a manner that allows the scheduler to schedule threads based on the periodic time interval (col. 9 lines 16-18).

21. As per claim 29, Fung teaches the invention as claimed, including a device as recited in claim 22, wherein after the scheduler is deactivated, the HAL further comprises computer-executable instructions for receiving a notification in response to an external event, the external event not being a system timer event (col. 8 lines 52-60), responsive to receipt of the notification, the HAL processing the notification in a manner that the scheduler remains deactivated for the dynamic variable amount of time (col. 9 lines 8-18).

Response to Arguments

22. **Applicant's arguments filed July 6, 2005 have been fully considered but they are not persuasive.**

23. Applicant submits that "*Toll teaches that an MT processor...may be used with any number of threads.*" Applicant argues that because "*the cited portions of Toll to [sic] not teach or suggest...doing anything at a 'predetermined periodic rate', a system of Toll may never 'scheduling one or more threads according to a predetermined periodic rate', as claim 1 recites.*"

24. What Applicant fails to address is that time-slicing, such that each thread in a system uses the processor for a predetermined period of time, is a well-known and conventional feature of multithreading (*See e.g.* Welland et al. (U.S. Patent No. 5,247,677, col. 4 lines 25-43)). Therefore, this technique of thread scheduling was prevalent at least as early as 1993. Threads may be scheduled in turn for a given period of time, i.e. at a predetermined periodic rate. At the expiration of the period, the thread yields control over the processor and another thread is scheduled. Some variation of this scheduling technique is used with every multithreaded processor. Toll is silent regarding time-slicing for at least two reasons: (1) time-slicing is so well-known and accepted in the art as a scheduling technique that to rehash its features would provide no insight into the operation of a multithreaded processor; and (2) the invention of Toll is directed to power conservation based on thread activity, such that the rate at which threads are scheduled is not relevant to the improvements provided. It is therefore submitted that Toll's failure to explicitly discuss time-slicing or scheduling threads at a "predetermined periodic rate" does not necessarily indicate that Toll does not support these features. Rather, they are so well-known and secondary to the object of the invention that it does not merit discussion.

25. Applicant submits that "*Toll teaches that an MT processor may turn off clocks in the processor responsive to threads entering a sleep state, and that internal clocks are turned back on responsive to a break event..*" Applicant relies on this teaching of Toll to argue that Toll fails to "*teach or suggest doing anything for 'a dynamic variable amount of time', as claim 1 recites.*" On this basis, Applicant argues that "*Toll may never 'deactivating one or more of the hardware elements and the program modules for a dynamic variable amount of time, the dynamic variable amount of time being independent of the predetermined periodic rate", as claim 1 recites.*"

26. First, it is noted that Toll does not use the specific language of "dynamic variable amount of time". The limitation is read as demonstrating that the hardware elements and/or program modules are deactivated for a period of time that varies on a case-by-case basis, i.e. dynamically. The hardware elements are thus deactivated and await a break event, which could occur at any point in time, and may vary depending on system conditions. The break event is not keyed to a system clock, as is a time-slice, such that activation in response to any internal or external event that is not correlated to a normal time slice is "independent" of the "predetermined periodic rate".

27. Applicant submits that "*Fung teaches that a power management unit switches to an active mode upon sensing hardware or software activity, and that during periods of inactivity, power consumption is reduced.*" Applicant argues that these teachings of Fung do not "*teach or suggest doing anything for 'a dynamic variable amount of time', as claim 1 recites.*"

28. This argument regarding the alleged deficiencies of Fung is very similar to the alleged deficiencies of Toll discussed in paragraphs 25-26. The discussion in paragraph 26 is hereby

incorporated by reference with respect to Applicant's arguments concerning Fung. That is, stating that hardware elements and program modules switch between an active mode and a power consumption mode in response to hardware or software activity is essentially the same as stating that they are deactivated for a "dynamic variable amount of time". That the exact language is not used is not convincing evidence that Fung fails to show these features. The amount of time that the computer may be in a period of inactivity could be very brief or very long. The exact amount of time is not precisely predictable, and therefore is a "dynamic variable amount of time".

29. The remainder of Applicant's arguments are similar to those presented above in paragraphs 23, 25, and 27. As these issues have been addressed, these arguments are also deemed to be not persuasive in view of the remarks in paragraphs 24, 26, and 28.

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J. Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T. An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
September 7, 2005